ABSTRACT OF THE DISCLOSURE

Conventionally, when an electric potential of a supporting substrate is fixed, there arises a problem in that impact ions are generated even in the vicinity of embedded insulating film in the proximity of a drain due to generation of a parasitic transistor using the supporting substrate as a gate so as to be likely to cause a parasitic bipolar operation. A method of the present invention includes the steps of: forming and patterning a LOCOS reaching an embedded insulating film, a gate oxide film, a well and a polysilicon film serving as a gate electrode; forming a second conductivity type high-density impurity region in an ultra-shallow portion of each of a source region and a drain region, a second conductivity type impurity region having a low density under the second conductivity type high-density impurity region of the ultra-shallow portion, and a second conductivity type impurity region having a high density under the second conductivity type impurity region having a low density and above the embedded insulating film; forming a sidewall around the gate electrode; forming a second conductivity type impurity region in each of the source region and the drain region; forming an interlayer insulating film and forming contact holes in the source region, the drain region and the gate electrode; and forming a wiring on the interlayer insulating film.